IN THE CLAIMS

63.   (Currently Amended) A microsequencer, comprising:

an instruction queue indexed by an instruction pointer and adapted to store instructions,

the instructions capable of being nested in a plurality of loop levels;

a plurality of loop counters adapted to store a remaining number of iterations associated

with an associated loop level; and

a plurality of loop instruction pointer registers associated with the loop counter and

adapted to store a loop instruction pointer value associated with a particular one of

the instructions marking the start of the associated loop level, wherein the

microsequencer is adapted to load the instruction pointer with the loop instruction

pointer value associated with [[the first]] a subsequent loop level in response to

the remaining number of iterations for the loop level equaling zero.

64.   (Original) The microsequencer of claim 63, further comprising a plurality of loop

count registers adapted to store a total number of iterations associated with an associated loop

level, and the microsequencer is adapted to load the loop counter associated with the loop level

with the total number of iterations when the particular one of the instructions marking the start of

the associated loop level is encountered.

65.   (Original) The microsequencer of claim 63, further comprising a repeat counter

adapted to store a repeat value indicating a number of remaining repeat iterations of a selected

one of the instructions.

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66. (Original) The microsequencer of claim 65, further comprising a repeat count register adapted to store a total number of repeat iterations associated with the selected one of the instructions.

67. (Currently Amended) A method for executing instructions, comprising:

storing a plurality of instructions in an instruction queue indexed by an instruction

pointer;

identifying a first instruction marking the start of a first loop, the first instruction having a

first loop instruction pointer value;

storing a remaining number of iterations for the first loop in a first loop counter; and

loading the instruction pointer with [[the first]] a subsequent loop instruction pointer

value in response to the remaining number of iterations for the first loop equaling

zero.

68. (Original) The method of claim 67, further comprising storing the first instruction pointer value in a first loop instruction pointer register.

69. (Original) The method of claim 67, further comprising:

identifying a second instruction nested within the first loop and marking the start of a

second loop, the second instruction having a second loop instruction pointer

value;

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storing a remaining number of iterations for the second loop in a second loop counter;

and

loading the instruction pointer with the second loop instruction pointer value in response

to the remaining number of iterations for the second loop equaling zero.

70.   (Original) The method of claim 67, further storing a total number of iterations

associated with the first loop in a first loop count register.

71.   (Original) The method of claim 70, further comprising:

identifying a second instruction marking the end of the first loop; and

loading the first loop counter with the total number of iterations when the second

instruction is first encountered.

72.   (Original) The method of claim 67, further comprising:

identifying a second instruction to be repeated;

storing a repeat value indicating a number of remaining repeat iterations for the second

instruction in a repeat counter; and

repeating the second instruction and decrementing the repeat counter until the number of

remaining repeat iterations for the second instruction equals zero.

73.   (Currently Amended) The method of claim [[67]] 69, further comprising:

storing a total number of repeat iterations associated with the second instruction in a

repeat count register; and

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loading the repeat counter with the total number of iterations in response to first encountering the second instruction.

75.   (Currently Amended) A microsequencer, comprising:

means for storing a plurality of instructions;

means for indexing the instructions using an instruction pointer;

means for identifying a first instruction marking the start of a first loop, the first instruction having a first loop instruction pointer value;

means for storing a remaining number of iterations for the first loop; and

means for loading the instruction pointer with [[the first]] a subsequent loop instruction pointer value in response to the remaining number of iterations for the first loop equaling zero.

76.   (New) An apparatus, comprising:

a microsequencer adapted to queue a plurality of instructions using an instruction queue indexed by an instruction pointer, said microsequencer to nest said instructions in a plurality of loop levels and store said instructions, said microsequencer also being adapted to store a remaining number of iterations associated with a corresponding loop level and marking the start of a loop level by storing a loop instruction pointer value associated with a particular one of said instructions.

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77.   (New)   The apparatus of claim 76, further comprising a plurality of loop instruction pointer registers associated with said loop counter, said instruction pointer registers being adapted to store said loop instruction pointer.

78.   (New) The apparatus of claim 76, wherein said microsequencer is further adapted to load said instruction pointer associated with a subsequent loop instruction pointer value associated with said loop level in response to said remaining number of iterations for said loop level equaling zero.

79.   (New)   The apparatus of claim 76, further comprising a plurality of loop count registers adapted to store a total number of iterations associated with an associated loop level.

80.   (New) The apparatus of claim 76, wherein said microsequencer is adapted to load said loop counter associated with the loop level with the total number of iterations when said particular one of the instructions marking the start of the associated loop level is encountered.

81.   (New) The apparatus of claim 80, further comprising a repeat counter adapted to store a repeat value indicating a number of remaining repeat iterations of a selected one of said instructions.

82.   (New)   The apparatus of claim 81, further comprising a repeat count register adapted to store a total number of repeat iterations associated with said selected one of the instructions.